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Auxiliary Board for the Outer Tracker

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Abstract

The auxiliary board for the Outer Tracker supplies the low voltage (+2.5 V, -3.0 V, +3.0 V), fast and slow control signals to the OTIS and ASDBLR boards and transforms paralell electrical timing and status data from the OTIS into serial optical data (GOL). One auxiliary board will be used for every module end. It sits on the rim of the outer tracker modules and is connected to the service box on the frame and the OTIS boards being plugged into it.

1 Parts

A list of connectors and ICs used on the auxiliary board is shown in table 1. The GOL is a Gigabit Optical link ASIC, specified in [1]. It receives 32 bits in paralell at 40 MHz from four OTIS chips. The data is serialized and 8/10 bit encoded. The GOL has a laser driver output sending data at 1.6 Gbit/s over a VCSEL diode. The VCSEL diode is a commercial product proved to be rad hard by the CMS calorimeter groups (HCAL, ECAL) [5]. The QPLL [2] will be necessary to reduce jitter to meet the requirements of the GOL. It comes along with a quartz oscillator. The rad hard power regulators L4913 for positive power and L7913 for negative power have an adjustable output voltage. Mind that the metal cooling surface on the package is internally connected to power and must be insulated when pressed against metal cooling bars. The connectors going off the module are a 8 pin RJ45 connector for the TFC, a 8 pin RJ45 connector for the Monitor signals, two 4-pin RJ11 connectors for I^2C.
Discussion: Shall we merge the 8-pin TFC connector and the 8-pin Monitor connector into one 30-pin connector? The 30 pin connector/cable is CERN stock.

function	name/part number	size(WxHxD)[mm^3]
connector for TFC signals	8-pin RJ45 Lumberg P137 S	15.74x12x18.35
connector for power-, temperature monitoring	8-pin RJ45 Lumberg P137 S	15.74x12x18.35
power connector	4-pin AMP Mate-N-Lok 5.08 mm pitch	25.5x?x13
laser VCSEL	Honeywell HFT 2291-541	13.33x8.89x21.44 +mounting
control LEDs ($\geq$14)	14 pieces 2X4(Farnell)	28x4+(6-10)x4
Hex switch for module location address	KDR-16H	10x10x12.4
I^2C bus connectors	2 * 4-pin RJ11 Lumberg P131 S	15.75x11.5x18.29
power regulator +2.5 V	1 * L4913 (SO-20)	12.95x2.65x10.55
power regulator +3.0 V	1 * L4913 (SO-20)	12.95x2.65x10.55
power regulator -3.0 V	1 * L7913 (SO-20)	12.95x2.65x10.55
serializer	GOL 1.0 144 L-fpBGA	13.0x1.63x13.0
de-jitter	QPLL(LPCC-28)	5?x?x5?
quartz	CC1F-T1A	8.0x1.75x3.7
OTIS board connectors	SAMTEC ZML-140-54-G-D-530-SM	53.98x13.46x9.27
reset push button		?x?x?

Table 1: Connectors and ICs needed for the auxiliary board

The connector to the OTIS board is a 80 pin SMD connector from SAMTEC. The fact that connectors to the OTIS are placed on top and bottom side of the board may lead to increased soldering prices.

1.1 Power regulators

The low voltage power regulators L4913 [4] for positive and L7913 for negative voltage are adjustable types. The input voltage is +5 V or -5 V. The estimated power consumption is shown in table 2. Table 3 shows the connectivity of the power regulators for the SO-20 package. The resistive divider is R1 between Vout and ADJ and R2, R3 (paralell) between ADJ and ground. For R1=1 kOhm R2 and R3 must be 1 kOhm, 22 kOhm for Vout=+2.5 V and R2=1 kOhm and R3=2.2 kOhm for Vout=3 V and Vout=-3 V, see figure3, 1000 nF capacitors to ground are recommended for the Vout pins.

If the 100 kOhm resistors R190-192 are used the maximum output current will be reduced to 40 percent of the the 4.5 A default value, which is too low for regular operation, since only 66 percent of the maximum current can be used.

Component	Number /aux-card	Power / Comp	Heat / Box
ASD-BLR	16	420 mW	6.7 W
pull-up resistor network	128	15 mW	1.9 W
OTIS	4	550 mW	2.2 W
GOL	1	390 mW	0.4
Others			1 W
L4913ADJ L7913ADJ	2 1		10 W
Total			22 W

Table 2: Power consumption on the auxiliary card

Pin Number in SO-20 slug up	Pin Name	Pin function	connectivity
1	Gnd	ground	Gnd
2	NC	not connected	not connected
3	NC	not connected	not connected
4	Vin	supply Voltage	+-5 V
5	Vout2	out half power (right Vin)	-3 V, +3 V, +2.5 V
6	Vout2	out half power (right Vin)	-3 V, +3 V, +2.5 V
7	SH-cntrl	short circuit valve controlling	100k pull up
8	OCM	short circuit monitoring	LED 2-4
9	NC	not connected	not connected
10	Gnd	ground	Gnd
11	Gnd	ground	Gnd
12	inh	inhibit	Gnd
13	ADJ	ADJ (adjustable vers.)	resistive divider +100 nF
14	SENSE	sense output	XV monitor
15	Vout1	out half power (left Vin)	-3 V, +3 V, +2.5 V
16	Vout1	out half power (left Vin)	-3 V, +3 V, +2.5 V
17	Vin	supply Voltage	+-5 V
18	NC	not connected	not connected
19	NC	not connected	not connected
20	Gnd	ground	Gnd

Table 3: Power regulator pin out

1.2 GOL 1.0

Table 4 shows the connectivity of the GOL 1.0 on the auxiliary board. The GOL 1.0 is packaged to a 144 L-fpBGA. It is used in 32 bit 8B/10B Gigabit Ethernet mode. The serial output is connected via a current divider to a VCSEL diode: from the GOL ld_cathode output to +2.5 V R=100 Ohm, from GOL ld_cathode output to the VCSEL input R=22 Ohm. The laser output current should be adjusted to 30 mA (I_bias). The laser driver bias current pins go to jumpers in order to try different settings. Until the best phase relation to the OTIS is found the conf_negedge pin is jumpered too. For the clock input the following possibilities are given:

- selectDiff = 1 (J101), differential clock from QPLL is used
- selectDiff = 0 (J101), solder jumper J102 to quartz, 40 MHz on-board quartz is used
- selectDiff = 0 (J101), solder jumper J102 to quartz and connector, 40 MHz on board quartz is used, clock can be used for monitoring (J111) and other boards
- selectDiff = 0 (J101), solder jumper to connector, external clock can be fed in (J111).

JTAG boundary scan can be performed via a minimized JTAG-connector (S103). The ready signal is connected to LED1. Reset_b is a active low master reset connected to $\overline{PwrUpRst}$ (the OTIS reset is active low too). The I^2C bus is distributed over the service box (see 2.3). The power for the GOL 1.0 is +2.5 V all inputs are 5 V tolerant.

Pin Number 144 L-fpBGA	Pin Name	Pin function	connectivity	level	inout
G2	cav/tx_er	data type	Gnd	CMOS	in
D10	clkLHC	40.08 MHz input clock	quartz	CMOS	in
D11	clkLHCn	diff 40.08 MHz clock n	ClkPll_n	LVDS	in
C12	clkLHCp	diff 40.08 MHz clock p	ClkPll_p	LVDS	in
C2	conf_glink	1:G-link, 0:8B/10B	Gnd	CMOS	in
G4	conf_i_ld<0>	laser driver bias current	J107	CMOS	in
H2	conf_i_ld<1>	laser driver bias current	J106	CMOS	in
B4	conf_i_pll	selects PLL bias current	+2.5 V	CMOS	in
D2	conf_laser	1:laser driver, 0:line driver	+2.5 V	CMOS	in
D12	conf_negedge	1:falling clk, 0:rising clk	J105	CMOS	in
E2	conf_wmode16	1:16-bit, 0:32-bit	Gnd	CMOS	in
F1	dav/tx_en	data type	+2.5 V	CMOS	in
L3-L5,M5,M6,	din<0-31>	input data	OtisN_D_p<0-7>	CMOS	in
L7,M8,M9,L9,				CMOS	in
K9,K10				CMOS	in
J10,J11,				CMOS	in
H11,G11,F12,				CMOS	in
K5,M4,K6,L6,				CMOS	in
M7,K7,L8,K8,				CMOS	in
M10,L10,K11,				CMOS	in
K12,J12,H12,				CMOS	in
G12,F11,				CMOS	in
E11	FF	ff1/ff0 G-link mode only	Gnd	CMOS	in
F10	flag<0>	flag bit<0> G-link only	Gnd	CMOS	in
E12	flag<1>	flag bit<1> G-link only	Gnd	CMOS	in
B5	i2c_addr<1>	I2C device address	Gnd	CMOS	in
A5	i2c_addr<2>	I2C device address	+2.5 V	CMOS	in
A4	i2c_addr<3>	I2C device address	LocAdr3	CMOS	in
C4	i2c_addr<4>	I2C device address	LocAdr4	CMOS	in
C3	i2c_addr<5>	I2C device address	LocAdr5	CMOS	in
D3	i2c_addr<6>	I2C device address	LocAdr6	CMOS	in
E1	JTAGTCK	JTAG clk (pull-high)	JTAG_pin5	CMOS	in
H1	JTAGTDI	JTAG data in (pull up)	JTAG_pin1	CMOS	in
G3	JTAGTDO	JTAG data out	JTAG_pin3	CMOS	out
G1	JTAGTMS	JTAG mode sel. (pull up)	JTAG_pin6	CMOS	in
A8	ld_cathode	laser driver output	LD_Cathode	30 mA	out
J3	ready	transmitter ready	GOL_ready	CMOS	out
D1	reset_b	master reset	$\overline{PwrUpRst}$	CMOS	in
K3	SCL	I^2C clock	I2c_Clk	CMOS	in
K4	SDA	I^2C data	I2c_Data	CMOS	in
C11	selectDiff	Sel. clock source (pull-up)	J101	CMOS	in
A7	serial_line_n	diff bit stream output	J108	?	out
A6	serial_line_p	diff bit stream output	J109	?	out
J2	test_analog	test output	J110	?	out
F2	test_shift	en. test of internal logic	Gnd	CMOS	in
A1...	VDD	+2.5 V power	+2.5 V	+2.5 V	in
A3...	GND	ground	Gnd	Gnd	in

Table 4: GOL 1.0 pin out

1.3 QPLL

Table 5 shows the connectivity of the QPLL on the auxiliary board. The QPLL is used as a jitter filter for the GOL 1.0 and the OTIS. Either 120 MHz or 160 MHz mode is usable, since only the 40 MHz outputs will be used. As a working basis we use the 160 MHz version (mode=1). The QPLL has LVDS as well as CMOS clock inputs. The LVDS inputs will be connected to the clock coming from the service box, where another QPLL sits, getting the input signal from the TTCrx. The QPLL comes in a LPCC-28 (5 mm x 5 mm, 0.5 mm pitch) package. The quartz is a CC1F-T1A from Micro Crystal Switzerland. Before custom quartz oscillators with 160.32 MHz are produced for the LHC detectors, 166.6286 MHz types will be employed. The quartz has an 8 * 3.7 * 1.75 mm^3 SMD package. The QPLL runs at +2.5 V.

Pin Number LPCC-28	Pin Name	Pin function	connectivity	level	inout
1	inLVDS-	diff clock input neg.	Clk_n (TFC)	LVDS	in
2	inLVDS+	diff clock input neg.	Clk_p (TFC)	LVDS	in
3	inCMOS	single ended clock	pull down	CMOS	in
4	externalControl	center freq. ext.	Gnd	CMOS	in
5	autoRestart	automatic PLL restart	+2.5 V	CMOS	in
6	reset	active low reset	$\overline{PwrUpRst}$	CMOS	in
7	f0Select< 3 >	frequency contr.	+2.5 V	CMOS	in
8	error	SEU error	QPLL_error LED 14	+2.5 V CMOS	out
9	locked	PLL status	QPLL_locked LED 13	+2.5 V CMOS	out
10	gnd	ground	Gnd	Gnd	in
11	vdd	+2.5 V power	+2.5 V	+2.5 V	in
12	lvds80MHz-	80 MHz clock output neg	n.c.	LVDS	out
13	lvds80MHz+	80 MHz clock output pos	n.c.	LVDS	out
14	f0Select< 2 >	frequency contr.	Gnd	CMOS	in
15	lvds160MHz-	160 MHz clock output neg	n.c.	LVDS	out
16	lvds160MHz+	160 MHz clock output pos	n.c.	LVDS	out
17	gnd	ground	Gnd	Gnd	in
18	vdd	+2.5 V power	+2.5 V	+2.5 V	in
19	lvds40MHz-	40 MHz clock output neg	ClkPLL_n	LVDS	out
20	lvds40MHz+	40 MHz clock output pos	clkPLL_p	LVDS	out
21	f0Select< 1 >	frequency contr.	Gnd	CMOS	in
22	vdd	+2.5 V power	+2.5 V	+2.5 V	in
23	cap	100 nF capacitor to Gnd	Gnd	Gnd	in
24	xtal1	Analog, Quartz crystal	to VCXO	?	inout
25	gnd	ground	Gnd	Gnd	in
26	xtal2	Analog, Quartz crystal	to VCXO	?	inout
27	mode	mode select 120 MHz(0) or 160 MHz(1)	J112	CMOS	in
28	f0Select< 0 >	frequency contr.	Gnd	CMOS	in

Table 5: QPLL pin out

1.4 Jumpers and push bottoms

Table 6 shows all jumpers for the current design. Jumpers have been introduced for (phase) clock choice, choice of the ASD board connected to the temperature sensor, choice between even and odd channels connected to the test pulse input and to define the laser driving current. Jumpers also allow the termination of the I^2C bus with alternative voltages. A Hex switch for the module location address has replaced the module location address connector.

function	jumper	default
sel_diff	J101	+2.5 V
clkLHC quartz/extern	J102	off
clkpll test pins	J103, J104	n.c.
conf_negedge	J105	?
conf_i_id1	J106	?
conf_i_id0	J107	?
serial_line_p (optical transmitter)	J108	off
serial_line_n (optical transmitter	J109	off
test_analog (GOL)	J110	off
clkLHC extern	J111	off
QPLL_mode 120/160 MHz	J112	+2.5 V
Testpulse even/odd	J201-J204	both
Temp sense board sel	J205-J208	?
last I^2C node	J209, J210	only last node connected
I^2C +2.5 V / +5 V /V_ext	J211, J212	+2.5 V
$\overline{PwrUpRst}$(active low)	SW1	+2.5 V
Hex Switch for Module Location Address	SW201	0001

Table 6: Jumpers on the auxiliary board

1.5 Laser VCSEL

The VCSEL diode is a commercial HFE2291-541 from Honeywell. It has been irradiated to $\geq$ 100 MRads with less than 14 % degradation [5]. It is packaged in a LC connectable plastic package. The voltage drop over the VCSEL is 1.8 - 2.2 V, the current modulation should be 7 mA.

2 Signals

The signals distributed over this board comprehend timing and fast control, I^2C, low voltage monitoring, test pulse for the ASD and TDC data from the OTIS. Table 7 shows the distribution of the signals over the connector pins to the service box on the detector frame. The power pins are described here too. Table 8 shows the connectivity to the OTIS board. LEDs signal the basic functionality of the components.

connector	signal	pin	in/out	level
TFC	L0Acc_p	1	in	LVDS
	L0Acc_n	2	in	LVDS
	L0Reset_p	3	in	LVDS
	L0Reset_n	6	in	LVDS
	BCntReset_p	4	in	LVDS
	BCntReset_n	5	in	LVDS
	Clk_p	7	in	LVDS
	Clk_n	8	in	LVDS
Monitor	+3.0 V mon.	1	out	sense
	-3.0 V mon	2	out	sense
	+2.5 V mon.	3	out	sense
	$\overline{PwrUpRst}$	6	in	CMOS
	TPulse_p	4	in	LVDS
	TPulse_n	5	in	LVDS
	Temp	7	out	sense
	Gnd	8	out	Gnd
Power	+5 V	1	in	power
	Gnd	2	in	Gnd
	Gnd	3	in	Gnd
	-5 V	4	in	power
Hex Switch for Module Location Address	LocAdr3	1	in	+2.5 V/Gnd
	LocAdr4	2	in	+2.5 V/Gnd
	LocAdr5	3	in	+2.5 V/Gnd
	LocAdr6	4	in	+2.5 V/Gnd
I^2Cbus in	Gnd	1	in	Gnd
	I2cData	2	inout	CMOS
	Gnd/V_ext	3	in	Gnd/Power
	I2cClk	4	in	CMOS
I^2Cbus out	Gnd	1	out	Gnd
	I2cData	2	inout	CMOS
	Gnd/V_ext	3	out	Gnd/Power
	I2cClk	4	out	CMOS

Table 7: Signal distribution on connectors to service box

signal	in/out	level	pin	pin	level	in/out	signal
+3 V	out	power	1	2	power	out	+3 V
Gnd	out	Gnd	3	4	Gnd	out	Gnd
-3 V	out	power	5	6	power	out	-3 V
Gnd	out	Gnd	7	8	Gnd	out	Gnd
+2.5 V	out	power	9	10	power	out	+2.5 V
OtisN_Adr0	out	CMOS	11	12	CMOS	out	OtisN_Adr1
OtisN_Adr2	out	Gnd	13	14	CMOS	out	LocAdr3
LocAdr4	out	CMOS	15	16	CMOS	out	LocAdd5
LocAdr6	out	CMOS	17	18	Gnd	out	Gnd
TestPad	out	CMOS	19	20	n.c.	out	NotConnect
I2c_Data	inout	CMOS	21	22	CMOS	inout	I2c_Clk
Gnd	out	Gnd	23	24	Gnd	out	Gnd
L0Acc_p	out	LVDS	25	26	LVDS	out	L0Reset_p
L0Acc_n	out	LVDS	27	28	LVDS	out	L0Reset_n
Gnd	out	Gnd	29	30	Gnd	out	Gnd
TPulseEv_p	out	LVDS	31	32	LVDS	out	TPulseOd_p
TPulseEv_n	out	LVDS	33	34	LVDS	out	TPulseOd_n
Gnd	out	Gnd	35	36	Gnd	out	Gnd
BCntReset_p	out	LVDS	37	38	LVDS	out	ClkPll_p
BCntReset_n	out	LVDS	39	40	LVDS	out	ClkPll_p
Gnd	out	Gnd	41	42	Gnd	out	Gnd
OtisND_n0(nc)	in	CMOSdiff	43	44	CMOSdiff	in	OtisND_p0
OtisND_n1(nc)	in	CMOSdiff	45	46	CMOSdiff	in	OtisND_p1
OtisND_n2(nc)	in	CMOSdiff	47	48	CMOSdiff	in	OtisND_p2
OtisND_n3(nc)	in	CMOSdiff	49	50	CMOSdiff	in	OtisND_p3
OtisND_n4(nc)	in	CMOSdiff	51	52	CMOSdiff	in	OtisND_p4
OtisND_n5(nc)	in	CMOSdiff	53	54	CMOSdiff	in	OtisND_p5
OtisND_n6(nc)	in	CMOSdiff	55	56	CMOSdiff	in	OtisND_p6
OtisND_n7(nc)	in	CMOSdiff	57	58	CMOSdiff	in	OtisND_p7
Gnd	out	Gnd	59	60	Gnd	out	Gnd
$\overline{PwrUpRst}$	in	CMOS	61	62	Gnd	out	Gnd
Otis_N_WPWrap	in	CMOS	63	64	CMOS	in	OTIS_N_RPWrap
TemMon_p	in	sense	65	66	sense	in	TemMon_p
TemMon_n	in	Gnd	67	68	n.c.	in	TemMon_n
Gnd	out	Gnd	69	70	Gnd	out	Gnd
+2.5 V	out	power	71	72	power	out	+2.5 V
Gnd	out	Gnd	73	74	Gnd	out	Gnd
-3 V	out	power	75	76	power	out	-3 V
Gnd	out	power	77	78	power	out	Gnd
+3 V	out	power	79	80	power	out	+3 V

Table 8: Signal distribution on connectors to the OTIS board the four OTIS boards connected to one auxiliary board are numbered 0-3, in the table N stands for this number.

2.1 Timing and Fast Control

Some TFC signals must be decoded in the service box, maybe the FPGA used for the SPECS implementation can decode the TFC signals for all LHCb sub-detectors. All TFC cables must have the same length of 4 m to minimize phase and timing problems. A reset signal ($\overline{PwrUpRst}$) directly issued by the ECS Specs is one of the signals on the Monitor connector. The GOL and QPLL resets will be connected to the $\overline{PwrUpRst}$ and a reset button (SW201). In order to perform a power up reset after the power is switched on, a capacitor is connected to the $\overline{PwrUpRst}$ signal, delaying the reset.
The L0Reset is used by the OTIS to reset the L0 pipeline and the de-randomizing buffer pointers, to adapt programmed parameters. It is decoded by the SPECS FPGA from TFC channel B broadcast. The bunch crossing ID reset BCntReset is used to restart the bunch crossing counters, it is directly issued by the TTCrx.

2.2 Monitoring and LEDs

The temperature and the low voltage are monitored with the help of a rad hard ADC on the service box. Functionality of the power regulators, the GOL, the QPLL and the OTIS are indicated by LEDs and Test Pulses can be send to check the functionality of the ASDs. Mind that the Gnd on the Monitor connector must not be connected to the service box ground, but only to the ADC inputs to avoid ground loops. The temperature sensor should be PT1000 or NPC10000. The temperature sensor net is connected to all four connectors going to the OTIS boards in order to be able to sense on either ASD board. All three voltages are sensed. The test pulses for the ASD preamplifier can be jumpered to the even and/or the odd test inputs, default setting is to pulse all ASD channels. The first four Led signals are the ready bit of the GOL 1.0, power up for +2.5 V, +3 V, -3 V. The OTIS [3] has two status pins called WPWrap and RPWrap, both of which are connected to LEDs. Table 9 shows the usage of the OTIS debug pins. The OTIS can drive 20 mA LED current (use $\geq$100 Ohm resistors.) Another two LEDs will be used for the QPLL_locked and QPLL_error. This results in 14 LEDs on the auxiliary board (table 10). The LEDs are 2X4 mm types that can be ordered at Farnell. They will be seated on 1/10 inch pitch sockets behind the power connector, and near the OTIS connectors see figure 5. Mind that the diode voltage drop is 1.6 V for the red LEDs, 2.2 V for the green ones. It has been verified that even the yellow and green diodes are clearly visible connected to 2.5 V over a 100 Ohm resistor. The temperature monitoring can only be done for one out of eight connected ASD boards. The selection

of the ASD board to be monitored is done via jumpers.

Debug-Mode[5:3]	Run Time Information	WPWrap	RPWrap
3′b000	Zero crossing of memory write and read pointer	Write pointer Write pointer	Read pointer Read pointer
3′b001	Zero crossing of de-randomizing buffer pointer	Write pointer Write pointer	Read pointer Read pointer
3′b010	Memory self test	Self test busy	Self test failure
3′b011	Read out sequence	Start of sequence	End of sequence
3′b100	De-randomizing buffer fill level	Buffer empty	Buffer full

Table 9: OTIS status information

LED	color	signal
1	green	GOL_ready
2	green	+2.5 V
3	green	+3.0 V
4	green	-3.0 V
5	green	OTIS0_WPWrap
6	red	OTIS0_RPWrap
7	green	OTIS1_WPWrap
8	red	OTIS1_RPWrap
9	green	OTIS2_WPWrap
10	red	OTIS2_RPWrap
11	green	OTIS3_WPWrap
12	red	OTIS3_RPWrap
13	green	QPLL_locked
14	red	QPLL_error

Table 10: LED assignment

2.3 I^2C

The I^2C serial bus supplies slow control signals to the OTIS TDC and GOL 1.0 (and optional further components in the service box). The bus has an input and an output connector for each board, so the nine boards belonging to one service box can be connected to the neighbor (accept for the first). The Hex Switch for the Module Location Address sits on the front of the board allowing to set the module location address for an built in module with a screwdriver (and some luck). It is planned to add another 6 module location address bits for station, layer and quarter so to define a unique module address in the Outer Tracker [6].
The three LSBs are hardwired on the auxiliary board to define the address for the GOL and the four OTIS chips (see below).
The GOL 1.3 manual states, that the I/O of the GOL 1.0 is TTL and +5 V CMOS tolerant, OTIS I/O will be implemented similar starting from OTIS 1.1. Nevertheless the level of the I^2C I/O should be adjusted on the service box. A jumper allows +2.5 V, +5 V or V_ext (coming over the I^2C connectors) pull ups on the auxiliary board for the last auxiliary board in the I^2C chain. The I^2C address space available on one bus (7bit address) is enough for the components on 9 detector module halves (4 OTIS + 1 GOL each), plus possible I^2C nodes on the service box. The OTIS uses only one I^2C address each while the GOL uses two consecutive I^2C addresses (for pointer and data). As the I^2C protocol reserves address 0 to 7 and 120 to 127 for system calls, they mustn't be used as device address. Table 11 shows how to split up the addresses for each I^2C chain (one each service box). The Two LSBs (0,1)are used to choose one out of four OTIS chips on a axillary board. Bit 2 (the third) is used to choose between GOL (1) or OTIS (0). The MSBs 3-6 are used to select one of the auxiliary boards, starting from 0001 going to 1001, 0000 and 1111 are reserved for the system, the remaining address space 1010-1110 can be used on the service box. The OTIS chip as well as the GOL chip have internal pull downs on all I^2C address inputs, so the address lines must be left open for low and pulled to +2.5 V for high. This implies that the Hex switch for the location address has to use real logic. Since the I^2C bus is non differential, the cables and connectors will be shielded, the shield of the I^2Cbus in and the I^2Cbus out connector will be connected to each other.

Address bit	device	possible values
0-2	OTIS0	000
	OTIS1	001
	OTIS2	010
	OTIS3	011
	GOL pointer	100
	GOL data	101
3-6	aux-board 0-8	0001-1001
	reserved	0000 and 1111
	service box	1010-1110

Table 11: I^2C addresses

3 Physical implementation

The physical implementation is given by the global OT module design. Here the dimensions stated on 12th Dec 2002 figure 1:

- Outer dimensions 150 mm x 100 mm x 1.6(?) mm
- center of 80 pin OTIS board connector from corner 13 mm, 34.1 mm
- 7 drills of 3.2 mm diameter for board mounting, four drills at the corners:
  - for the OTIS board side 23 mm from long side, 5 mm from the short side
  - for the service board side 5 mm from long side, 5 mm from the short side

  three drills between the power regulators: 40 mm from service box side, 15 mm / 75 mm / 135 mm from the short side.

The size of the bigger parts is shown in table 1, their position is subject to the layout. As the power regulators have to be screwed to the cooling, they have a fixed position on the back of the board. With exception of two 80 pin OTIS board connectors and resistors R150-R152 all other parts are mounted on the upper side of the board. Figure 2 shows a drilling test for all front connectors.

Figure 1: GOL-auxiliary board overview, all units are mm.

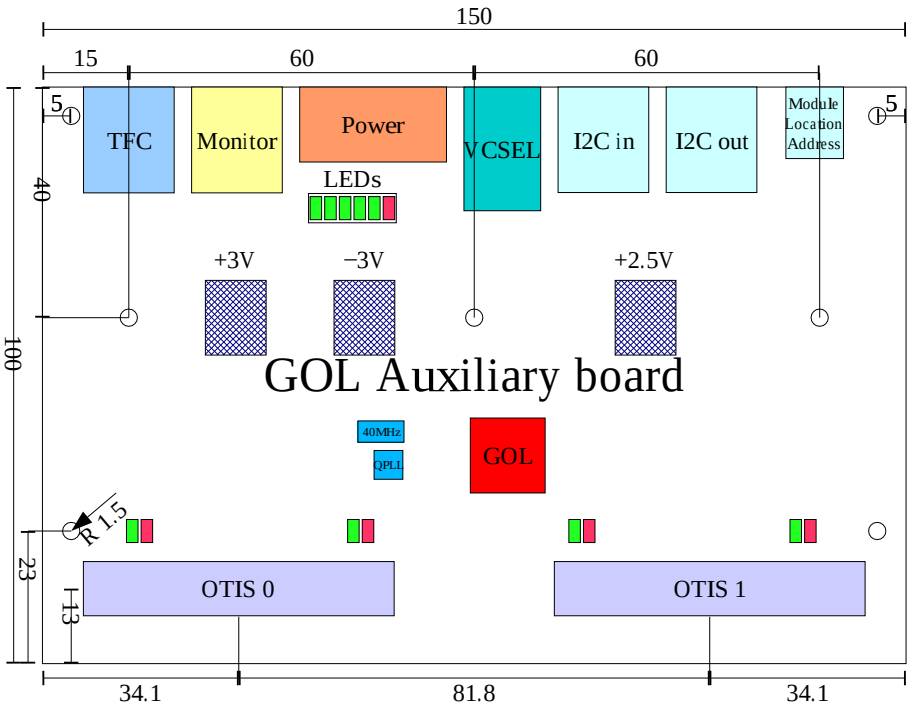
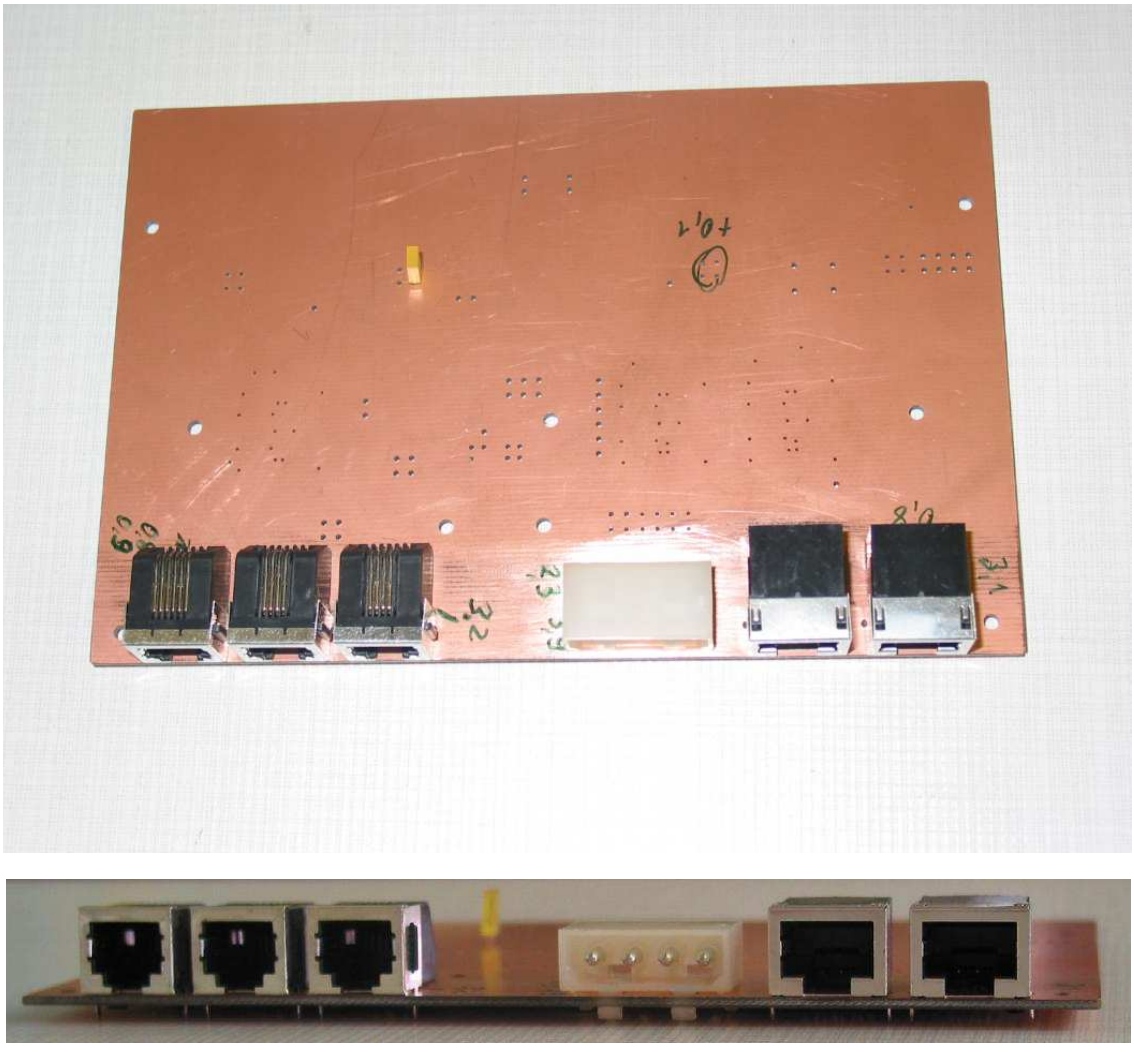


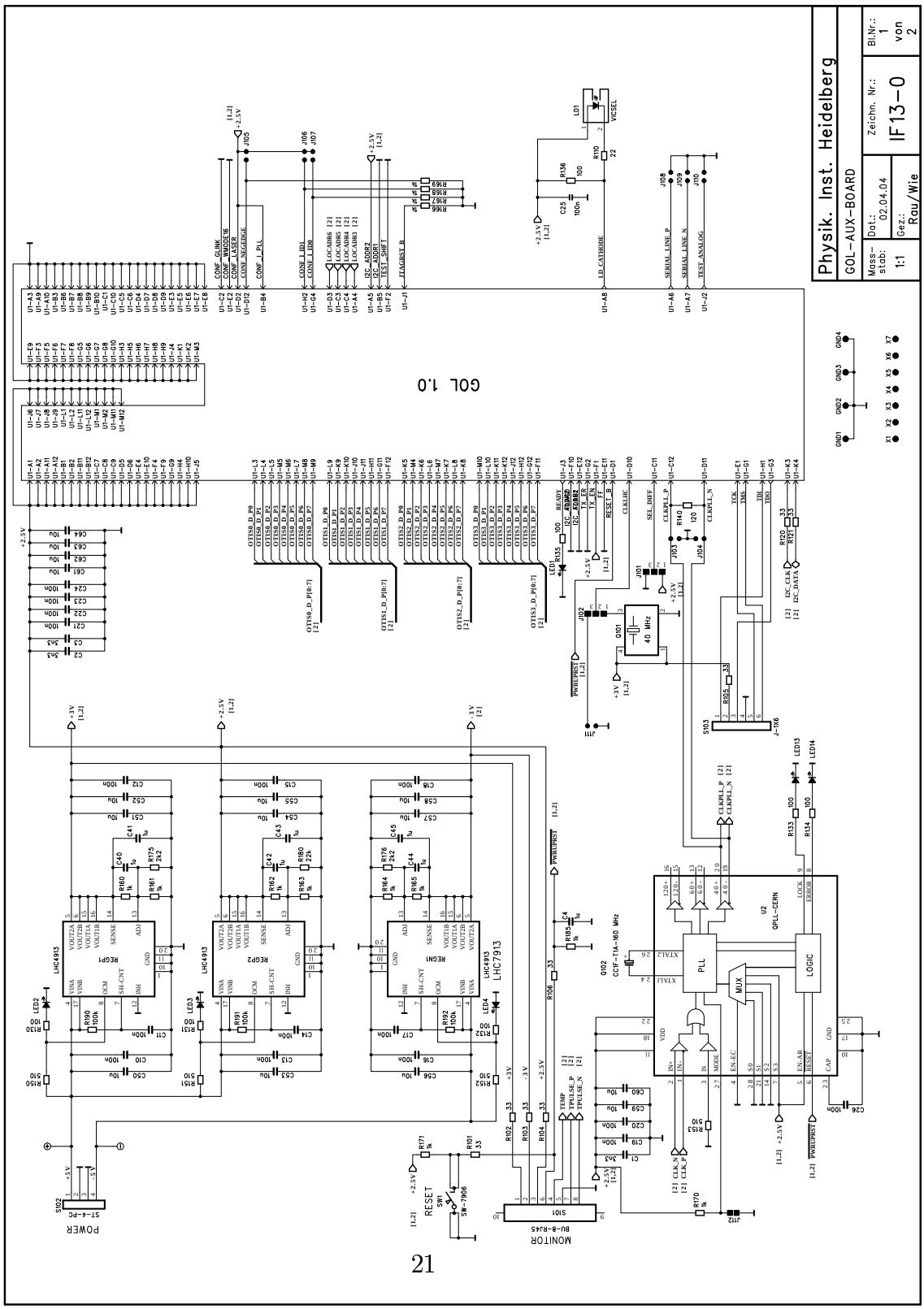
Figure 2: GOL auxiliary board drilling test



A Schematics

Figure 3 shows the schematics for the connectivity of the GOL 1.0, the QPLL, the power regulators, the power pins and the monitor connectors. Figure 4 shows the connectors for the OTIS boards, the I^2C bus (in and out), the local address and for the TFC signals. The component placement is shown in figures 5(top) and 6(bottom).

Figure 3: GOL-auxiliary board schematics (1/2)



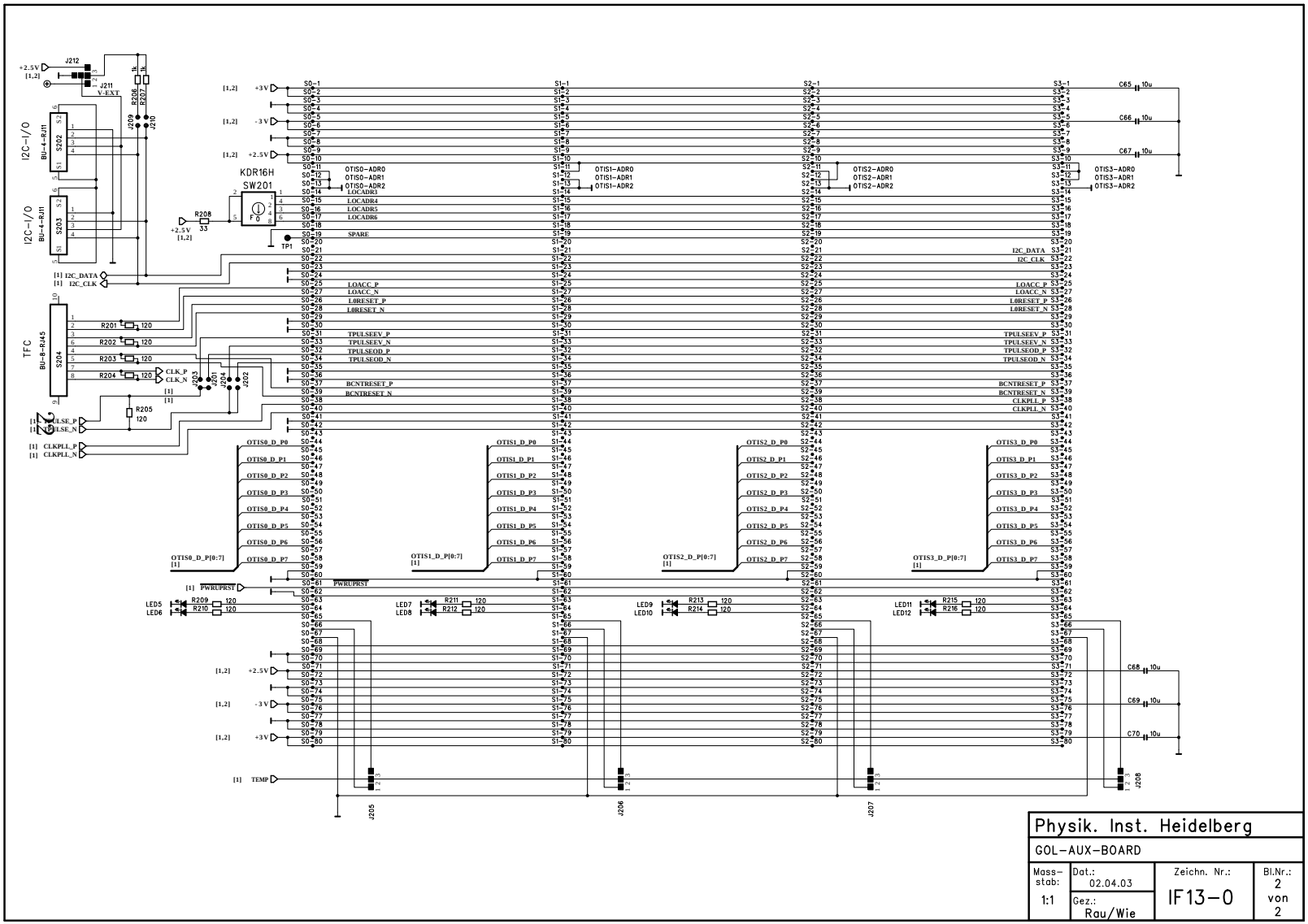


Figure 4: GOL-auxiliary board schematics (2/2)

Figure 5: GOL-auxiliary board component placement specification top (1/2)
DO NOT USE 100k resistors for R190-R192, because then the current limit is too low!

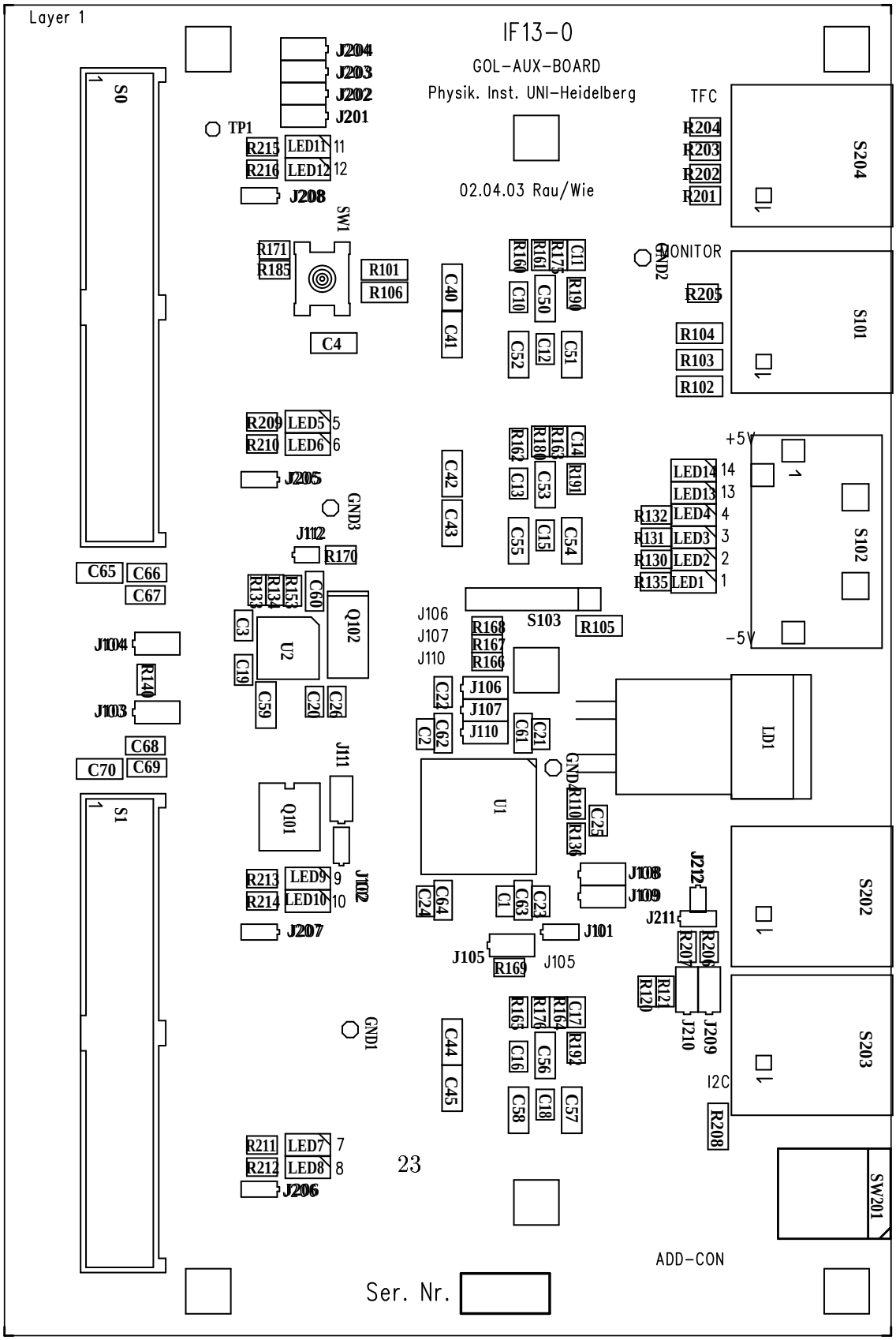
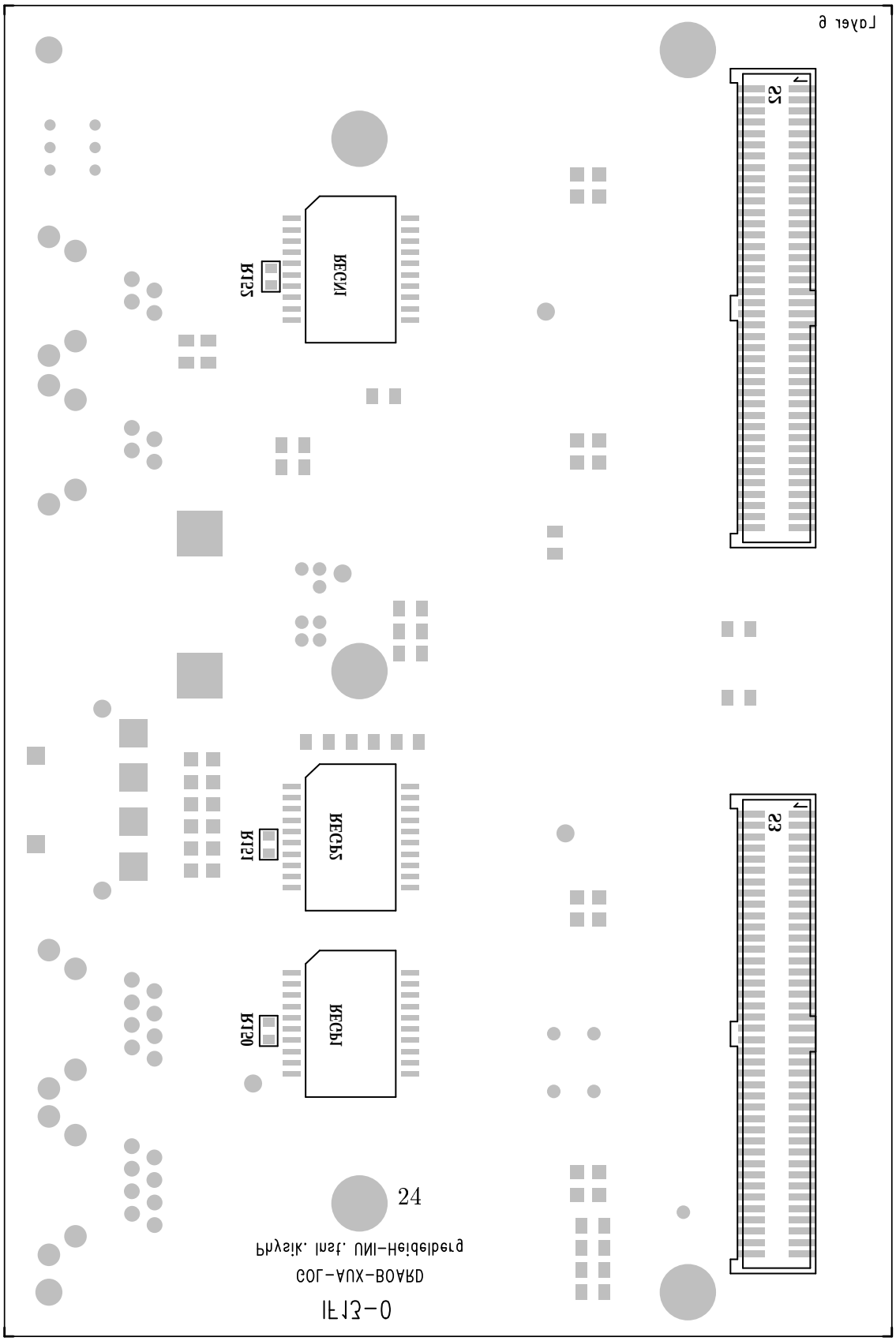


Figure 6: GOL-auxiliary board component placement specification bottom (2/2)



Contents

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