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TTCrx Setup in Heidelberg

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Abstract

The LHCb Outer Tracker group has developed the OTIS TDC for drift time measurements. In order to validate the communication between the OTIS TDC and the fast control system, especially the radiation hard TTCrx chip a test setup was made. It consists of a OTIS TDC, a TTCrx on a TTCrm Test board plus motherboard and a number of VME cards to generate the optical data for clock and trigger. A FPGA was added to the setup in order to validate the OTIS header and synchronize the OTIS data. In a final step the OTIS data was sent over a optical link.

1 Hardware

The units used for the setup are:

- Linux PC as user interface for the VME CPU
- RIO 8062 VME CPU to generate VME commands
- TTCvi as VME TTC interface
- TTCvx for clock generation and optical transmission
- TTCrx on TTCrm board, a rad hard TTC receiver
- motherboard for TTCrm power and LVDS line driver
- OTIS 1.0 on OTIS test board V2
- GOL EV2 board with ACEX 1K100 FPGA

The TTCvi [3], TTCvx [4] and TTCrm [1] boards are evaluation modules provided by CERN EP devision. They are used to simulate the timing and fast control environment used in the LHC experiment. While the TTCvx and TTCvi are only used for test setups the TTCrx will be used on the LHC detectors. The Linux PC and the RIO 8062 VME CPU are used to generate VME commands for the TTCvi. A user interface was written [5] to make the timing and fast control commands accessible via a context menu. The TTCvi interprets the VME commands and creates two data channels that are transmitted via the TTCvx. Channel A is used for L0 trigger broadcast while channel B can be used for encoding detector specific commands [6]. The data from channel A and B is serialized and transmitted optically by the TTCvx VME module. The TTCvx module is also used to create the 40 MHz clock signal. The optical fiber was a 50 m suner fibreoptics (50/125) type connected with ST connectors. A TTCrm mezzanine card sits on the receiving side of the optical fiber. The optical signals are received by an Agilent HFBR-2316T photo diode pre amplified and decoded by the TTCrx 3.1 chip. Alternatively an old ECP680-1102-610B TTCrm card from ATLAS was used. To supply power (5 V) and to convert the trigger, clock and the reset signal coming from the TTCrx from single ended 5 V LVTTL ? signal to LVDS a motherboard was made. The single ended LVTTL to LVDS conversion was performed by an DS90C031 LVDS Quad CMOS Differtial Line Driver (in a dual in line package). For the tests described in section 2 the power for the TTCrm cards came from a alternative motherboard, which had to be exchanged. The OTIS 1.0 full size prototype directly mounted on a OTIS Test board V2 was examined in the test described in 3. It was powered with 2.89 V instead of 2.5 V in order to compensate for the voltage drop over the inductivities L1, L2 on the test board. The 2.5 V were checked at the OTIS.

2 Clock distribution

Starting with a simple setup the clock distribution was checked for two different TTCrx cards, an old ECP680-1102-610B card from ATLAS and a newer TTCrm card with the TTCrx3.1 from LHCb OT. Figure **??** shows the setup. The clock output of the TTCvi goes to the TTCvx clock in. TTCvi direct outputs A and B (both ecl) are connected to the TTCvx channel A and B ecl-inputs. The TTCrx-board is connected to the TTCvx via 50 m suner fiber optics optical fiber (50/125) connected with ST connectors. A digital oscilloscope Tektronix TDS 782A was used to compare the TTCvx clock output with the TTCrx clock output. While the TTCvx clock output was

connected to the scope by a 50 ohm cable, the TTCrx clock was connected via an active 1.5 GHz probe. The persistence measurements show a average signal for 32 ms up to 10 s and indicates jitter problems.
The measurements showed better results for the newer TTCrx3.1 chip than for the ECP680-1102-610B test board. The following shots where taken:

- ECP680-1102-610B without persistence 1
- TTCrx 3.1 without persistence 2
- ECP680-1102-610B with 10 s persistence 3
- TTcrx 3.1 with 10 s persistence 4
- ECP680-1102-610B with 10 s persistence 1ns x-scale 5
- TTCrx 3.1 with 10 s persistence 1 ns x-scale 6
- TTCrx 3.1 with 32 ms persistence 1 ns x-scale 7

Figure 1: ECP680-1102-610B without persistence
The newer version of the TTCrx shows much less overshoot than the one on the ECP680-1102-610B board.

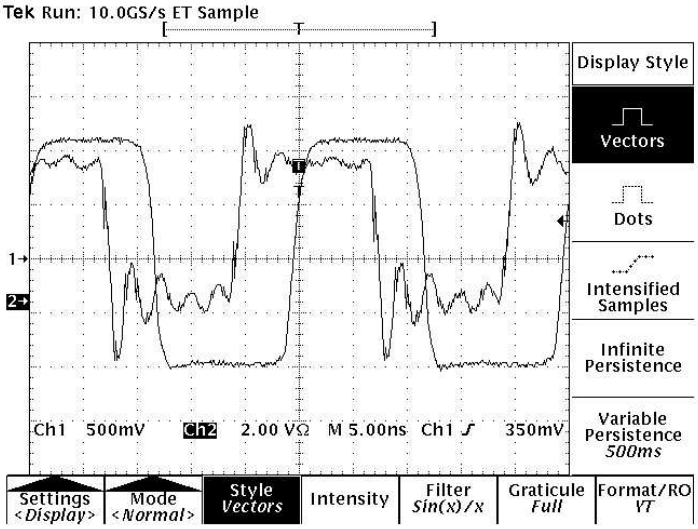


Figure 2: TTCrx 3.1 without persistence The newer version of the TTCrx shows much less overshoot than the one on the ECP680-1102-610B board.

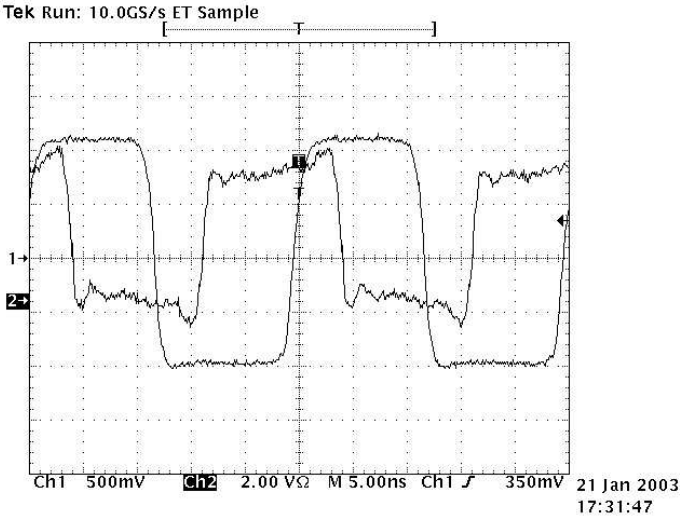


Figure 3: ECP680-1102-610B with 10 s persistence

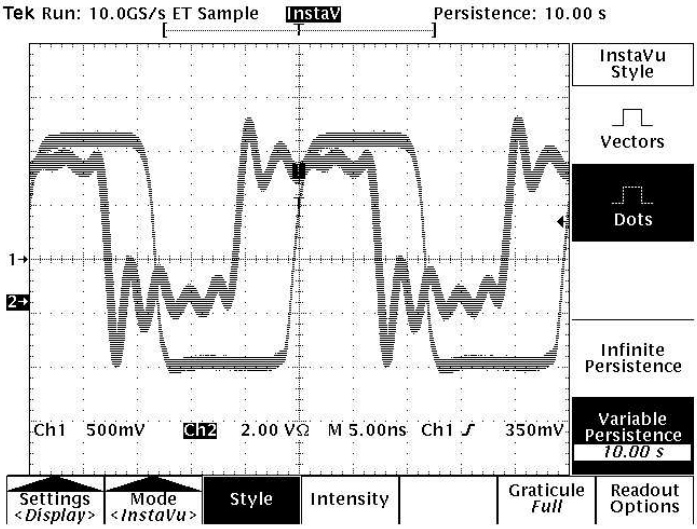


Figure 4: TTcrx 3.1 with 10 s persistence

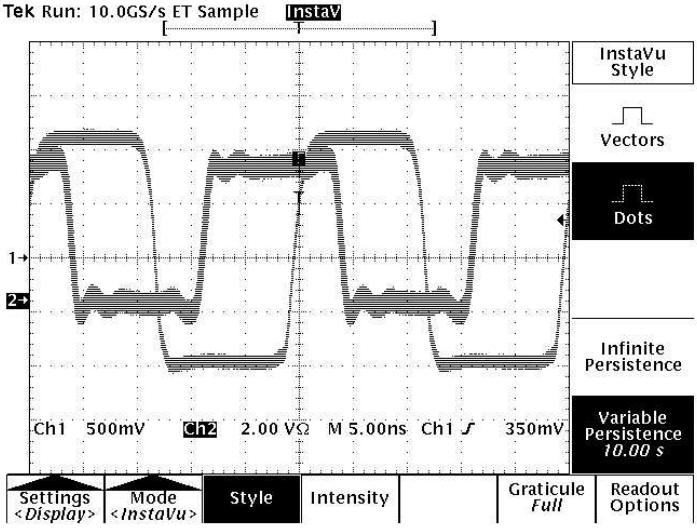


Figure 5: ECP680-1102-610B with 10 s persistence 1ns x-scale
The oscilloscope pictures with the 1 ns timescale indicate the quality of the phase relation between TTCvx output and TTCrx output. The ECP680-1102-610B board TTCrx shows 600 ps peak to peak jitter, whereas the TTCrx 3.1 on the TTCrm board shows 400 ps jitter.

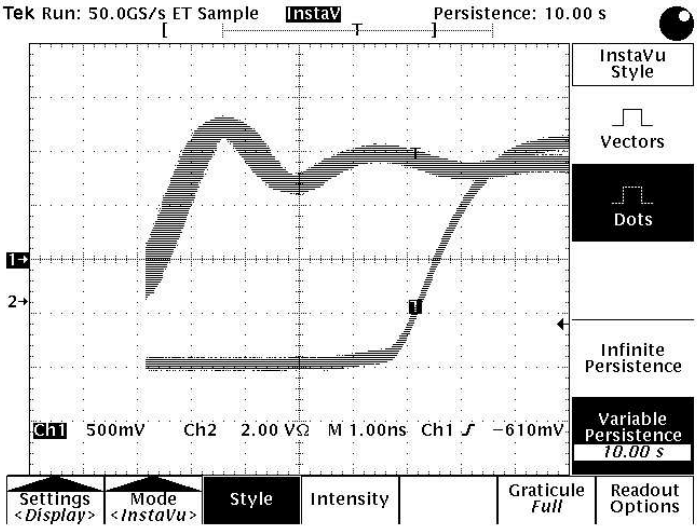


Figure 6: TTCrx 3.1 with 10 s persistence 1 ns x-scale

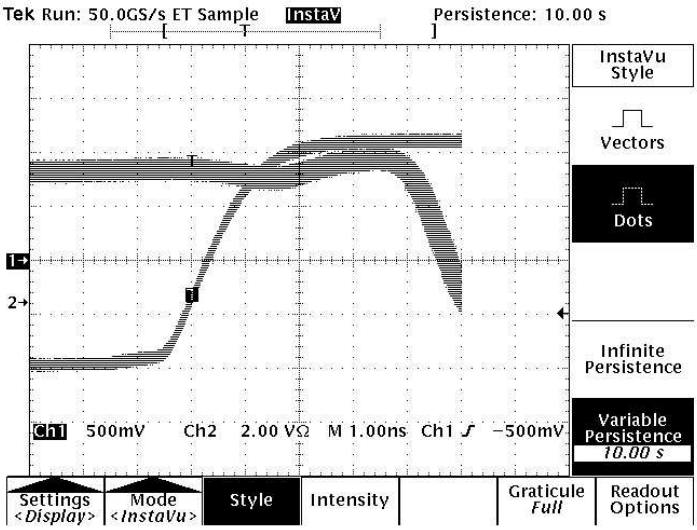
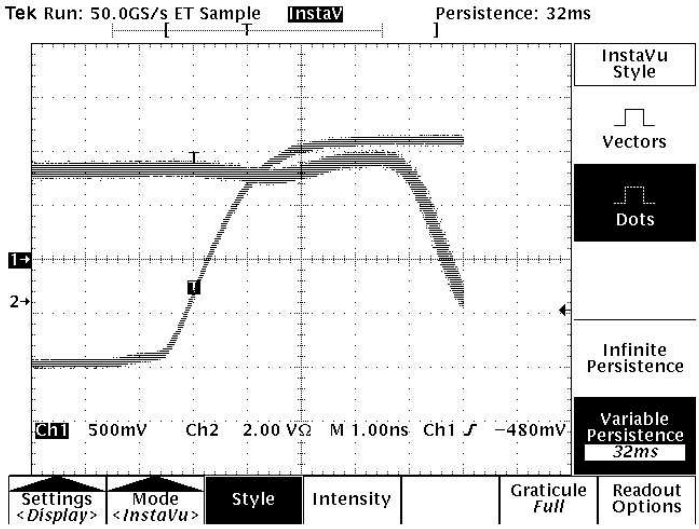


Figure 7: TTCrx 3.1 with 32 ms persistence 1 ns x-scale
At close look a dependance of the jitter measurement to the persistence time is visible



3 OTIS TTCrx test

To of the setup used in 2 a RIO VME CPU and the OTIS 1.0 TDC where added. In order to send all relevant TFC commands to the TTCrx a software interface was written [5]. The software makes it possible to easily set the random L0 trigger frequency or to initiate resets for bunch counter (being the OTIS fast reset). The TTCrm board was first plugged on an old motherboard being not very reliable (having a slack joint), then a custom board was assembled providing 5 V power and supporting the LVDS driver. The power up reset (Reset) for the TTCrx was delayed by soldering 50 Ohm serial and 47 μF in parallel to the Reset_b pin, thus ensuring a 5 ms delay for the reset signal in respect to the chip power. Figure 8 shows the setup.
Clock, L0 accept (L1Accept for the TTCrx) and the bunch counter reset coming from the TTCrx were connected to the inputs of the differential line driver and the corresponding outputs (terminated with 47 Ohms) via twisted pair cable to the OTIS see table 1.

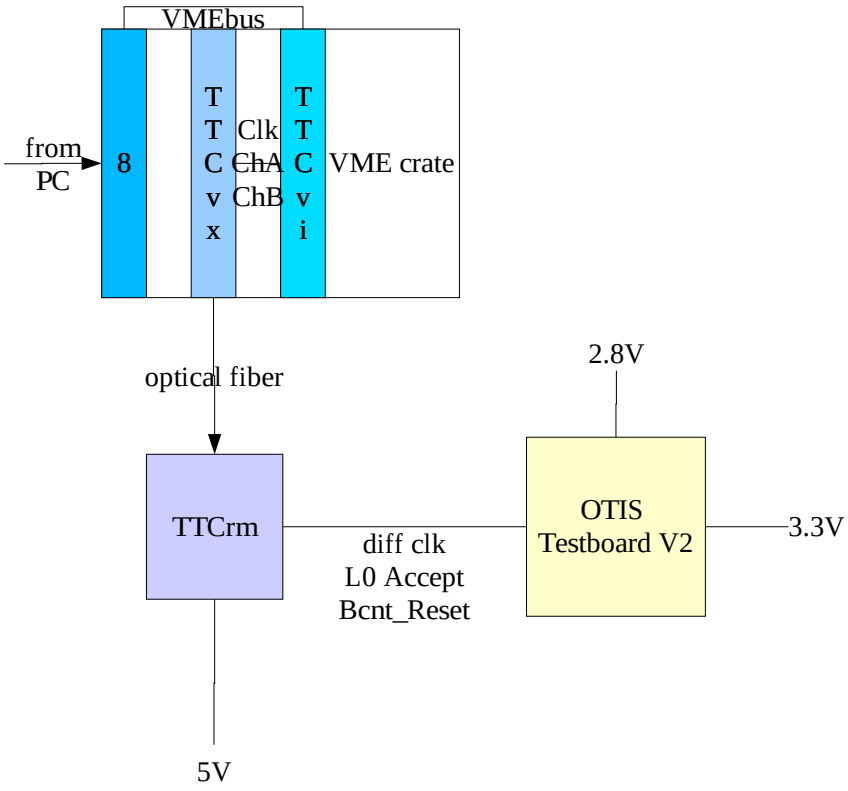
Signal	length [cm]	negative	positive	TTCrm	DS90C031	OTIS EV2
Clock	48	pink	red	J1-1	1,2,3	ID5, ID6
L1Accept	50	pink	white	J2-6	13-15	ID9-9,11
BcntRes	48	pink	orange	J2-9	9-11	ID9-5, 7

Table 1: Twisted pair connection between TTCrm and OTIS TDC

At first the OTIS 1.0 (on OTIS board V2 number 4) was clocked only. The clock can be observed at the last dummy out pin, where it showed no spikes. After the OTIS was properly reset by the bunch counter reset, the expected data could be observed at the data outputs. On the OTIS test board V2 the LVDS output data are converted to single ended data by a DS90LV032 line receiver. The OTIS data consists of an 32 bit header and 32 data bytes. The header starts with the OTIS ID, which can be alternated by jumpers on the OTIS test board V2. The OTIS ID could be clearly seen with a digital oscilloscope Tektronix TDS220. The data bytes are 1100 0000 for no valid hits, which was checked. The latency between L0 accept signal on the TTCrx and the OTIS data was measured to be 58 ns +-2 ns. The cable for the OTIS Data was 87 cm, the L1 Accept cable 58 cm
The following test were carried out (9.4.2003):

- voltage test on all boards
- qualitative signal tests

Figure 8: OTIS TTCrx setup
The OTIS is triggered, clocked and reset over the TTCrx chip as foreseen for the LHCb implementation



- OTIS signal tests

3.1 Voltage test on all boards

As the ASIC performance varies with the supplied voltage the power was checked for most inputs see table 2. All voltages were within the specified range. Mind that the voltage at the OTIS blocking was measured without operation.

pin	voltage [V]
TTCrm in	5
TTCrx blocking	3.3
OTIS V2 (5) 2.5 V in	2.9
OTIS blocking	2.65
OTIS diff. line Rec.	3.32
GOL EV2-0 2.5 V/3.3 V	2.46/3.29

Table 2: voltages measured at the TTCrx-OTIS setup

3.2 Qualitative signal tests

With the help of the oscilloscope the signals in table 4

signal	quality
TTCrm ClkDes1 J1-1	good
L1Accept TTCrm J2-6	good
BcntRes TTCrm J2-9	good
at DS90C031	
Clk pos (2)	good (1 V)
Clk neg (3)	good (1 V)
L1Accept pos (14)	good (4 V)
L1Accept neg (13)	good (3 V)
BcntRes pos (10)	good (5 V)
BcntRes neg (11)	o.k. (3 V)

Table 3: signals checked for the TTCrx-OTIS setup

3.3 OTIS signal tests

For five different OTIS chips on OTIS V2 boards the functionality was checked by monitoring the Last Dummy out clock signal on the oscilloscope, measuring the control voltage and checking the data output after a L1 Accept signal. The measured control voltages are shown in table **??**

Board number	V_control [V]
5	1.18
4	1.075 - 1.08
6	1.07
7	1.20
8	1.07

Table 4: DLL control voltage measured for 5 OTIS chips

The OTIS address was set to 1001 0000 0001 on the OTIS EV2 boards. On all five boards (4-8) the data pattern in table5 was identified (showing the expected values), X stands for 0/1 depending on the BX counter value.

output pin	binary values
4	000X 0...0
6	000X 0...0
8	000X 0...0
10	000X 0...0
12	010X 0...0
14	000X 0...0
16	000X 1...1
18	110X 1...1

Table 5: Data at OTIS outputs for OTIS EV2 boards 4-8

4 TTCrx OTIS FPGA tests

In addition to the TTCrx OTIS test setup described above a FPGA was added in order to validate the OTIS header continuously and to establish a program for the synchronization on the OTIS data that will be used on the L1 Read Out Board. The basic functions are to synchronize the OTIS data to the FPGA clock, to find the OTIS header, to check the 12 bit OTIS ID and to compare the BX value coming with the OTIS data to the internal counter.

4.1 Hardware

The GOL EV2 board was connected to receive the OTIS data. Only the FPGA ACEX 1K100 (ALTERA) but not the GOL 1.0 was used here. The clock was taken from the Last Dummy out pin of the OTIS EV2 board, L1 Accept and BXReset came directly from the TTCrm board. The Otis data was transmitted by a 20 pin flat cable.
The GOL EV2 board features 12 LEDs. With the help of three jumpers on J8 of the GOL EV2 the information to be displayed can be chosen. Table 6 shows the jumper settings.
The error count is the number of Bx numbers that had unexpected values. The intcount number gives the number in the FPGA bx counter. Founddiff is the difference between the internally generated, buffered Bx number and the Bx number from the OTIS. The bx trigger is the write strobe for the BX number found in the OTIS data, the packettrig (idflag) is the strobe for the OTIS ID extracted from the OTIS data. The internal variable act is low when the internal counter is zero. Lock shows the locked state of the state machine bxlock, locked diff shows the initial difference between internal counter Bx and OTIS Bx number.

4.2 Synchronisation algorithm

The synchronization algorithm comprehends the following parts:

- Data buffer for clock synchronization of incoming data
- header bit detection
- 8/16 bit deserialisation
- OTIS ID output
- Bunch counter extraction

jumper configuration	LED output
000	error count[11..0]
001	error count[31..20]
010	intcount[11..0]
011	intcount[31..20]
100	led[7..0] founddiff[7..0]
	led8 bxtrig (strobe)
	led9 packettrigger
	led10 act (active state)
	led11 lock (bxlocked)
101	led[7..0] currentbx[7..0]
	led8 bxtrig (strobe)
	led9 packettrig
	led10 act (active state)
	led11 lock(bxlocked)
110	otisid
111	led[7..0] lockeddiff
	led[10..8] 000
	led11 lock (bxlocked)

Table 6: Jumper settings for the LED display

- comparison of OTIS Bunch ID and internal BX counter

4.3 Clock Synchronisation to OTIS ID output

In the first part of the algorithm (program name step1v2) the OTIS data coming over a 20 pin fine pitch cable are buffered in an input flip flops in order to gain data sync to the internal chip clock. The incoming data bytes are checked for non zero bits and meanwhile stored in a second flip flop. If a high bit is found the data bytes are combined to 16 bit words starting from the byte with the first non zero value. The 12 bit OTIS ID is extracted and output for the full event length (36 cycles), together with a OTIS ID strobe. The 16 bit data words are output separately. The underlying state machine has three states: The listening state (initial state), the algorithm is waiting for a high bit. The active state, the algorithm has found an OTIS header and outputs the data for 36 cycles for the uneven bytes. The shifting state, the same as the active state but for the even bytes.

4.4 Bunch counter check

The BxExtractor delivers the BX number received with the OTIS data together with a strobe. It is followed by a state machine (Bxlock):

- locked (initial state), the difference between the internal counter (count32) and the OTIS Bx number is output,
- listening, it is waiting for the next Bx number from the BxExtractor
- counting, it waits 160 cycles after a BX reset.

After a Bx reset the internal counter is set to zero. In order to stay synchronous to the OTIS, the value of the internal counter is stored in a 16 word deep FIFO [1], when a L1 accept is broadcasted. The oldest entry in the FIFO is compared to the OTIS data Bx number (compare2). L1 Accept and counter data are both synchronized to the internal FPGA clock by input FIFOs, which implies together with equal cables length that the internal counter value is equal to the OTIS Bx counter.

4.5 Results

The synchronization algorithm is working as specified. The OTIS ID is displayed (jumper setting 110) correctly for the whole event length. The internal Bx counter and the OTIS Bx counter run synchronously for L1 Accept rates for 1.1 MHz (constantly), 100 kHz random and 1 Hz random.

5 TTCrx OTIS FPGA GOL setup

By adding the optical link to the previous setup, it was tried to recover the OTIS data under more realistic conditions.

5.1 Hardware

The optical link consisted of the GOL 1.0 serializer, a VCSEL diode, 5 m optical fiber and the TLK2501 Ev board see table 7. For some tests an external pulse generator HP 8082A was used. A drawing of the setup is shown in figure 9. Figures 10 to 14 show pictures of the lab setup.

[1] the OTIS derandomizing buffer is the equivalent of this FIFO

function	product
serializer	GOL 1.0
optical transmitter	HFT2291-541 VCSEL diode
optical fiber	Krone 7006-2688-15
optical receiver	Stratos MLC-25-b-1-TL
deserialiser	Texas Instruments TLK2501 on Evo board

Table 7: Hardware components of the optical link

5.2 Recovering OTIS data after the optical link

In the LHCb experiment the OTIS data will be serialized (32 bit @ 40 MHz to 1 bit @ 1.6 MHz) and send over optical fiber to the off detector electronics (ODE). There the data is deserialised to 16 bit @ 80 MHz and input to FPGAs. It is important to use the same master clock for the sending and the receiving side, otherwise frequency differences will lead phase shifts resulting in data loss. As the GOL 1.0 serializer could not use the clock distributed by the TTCrx 3.1 it had to be run with a more stable clock. All test where performed with the TTCrx 3.1 sending clock, BcntRes and L1Accept to the OTIS 1.0 and the FPGA. The GOL 1.0 was reset with the TTCrx BcntRes but clocked by an on board quartz or an external pulse generator (in both case the FPGA was used to create 40 MHz for the GOL 1.0 from 80 MHz input frequency). The TLK 2501 had to be clocked from the same clock as the GOL 1.0. For easier evaluation the data bytes from one OTIS were input to two consecutive inputs of the GOL, leading to an output of that byte at 40 MHz at the TLK (loosing half the bandwidth). The data bytes output at the TLK where input to the same FPGA, in order to recover the OTIS data as in the above section.
It could be shown that at least for two thirds of the events the OTIS header could be recovered correctly, while the remaining events where errorous. It is assumed that this is because usage of different clocks could not fully be compensated by input and output FIFOs on the FPGA. In tests to come the GOL 1.0 will work with the global clock filtered by an additional QPLL chip. Additionally the FPGAs which will be used in the later L1 common buffer boards will have extra PLL clocks for the data stream from the TLK chips.

Figure 9: TTCrx OTIS FPGA GOL drawing

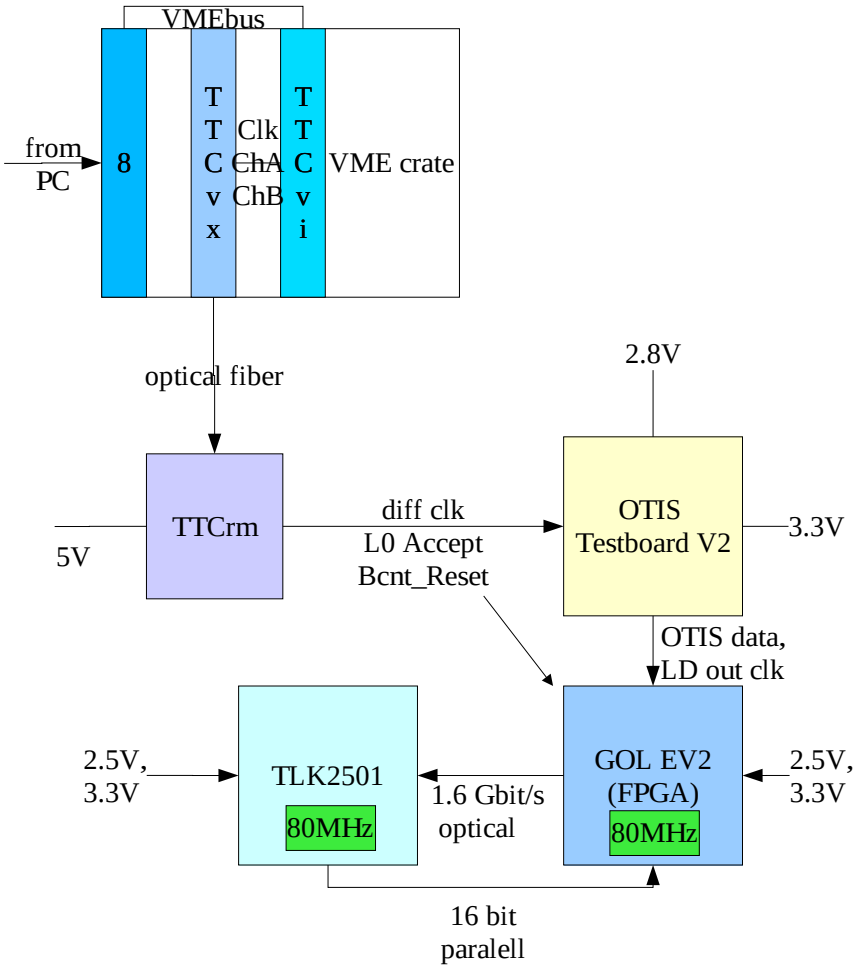


Figure 10: TTCrx OTIS FPGA GOL setup

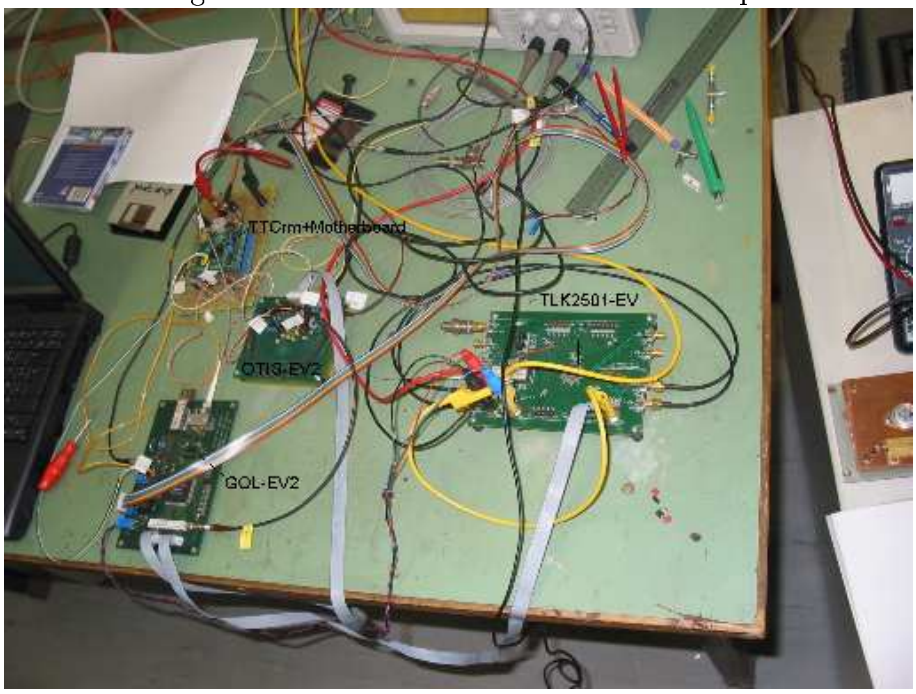


Figure 11: TTCrm and Motherboard

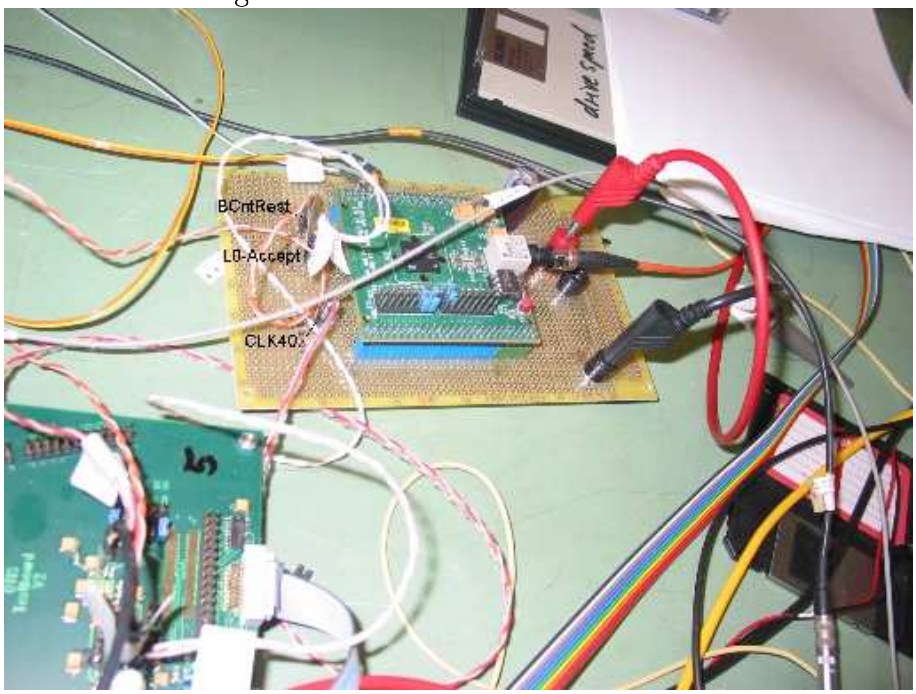


Figure 12: OTIS EV2 board

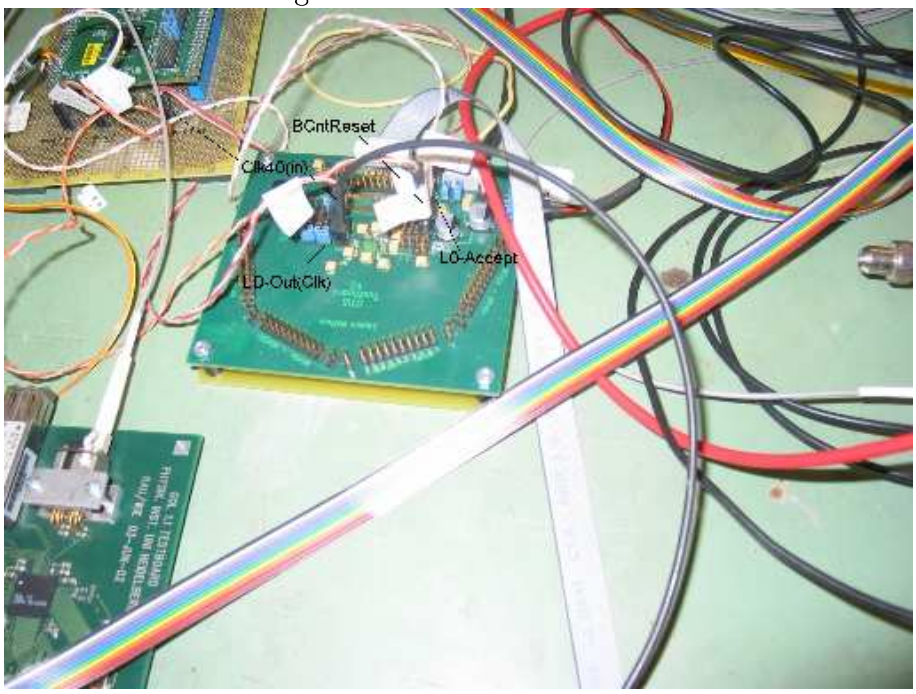


Figure 13: GOL EV2 board

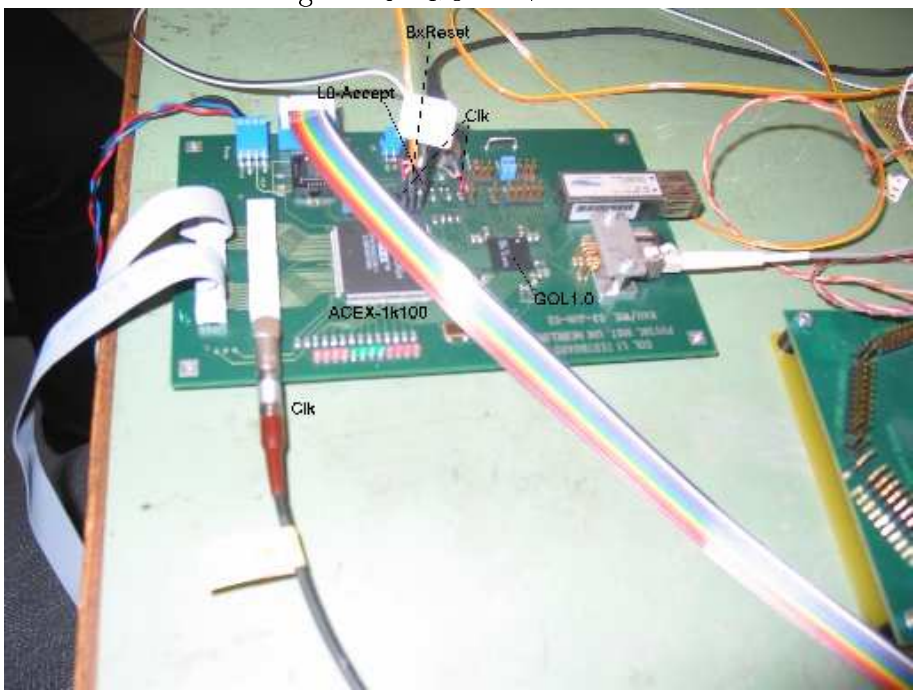
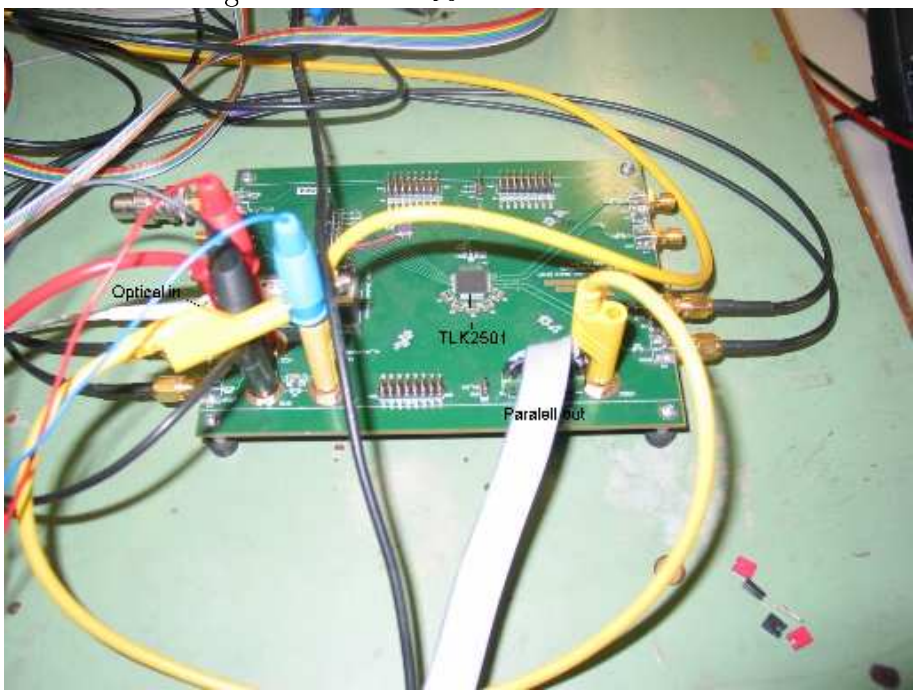


Figure 14: TLK2501 Evaluation board



Contents

List of Tables

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