

Address Scheme for the Outer Tracker FE Electronics

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Abstract

The document proposes an address scheme for the Outer Tracker Front End Electronics which can be deduced in a unique way from the geometrical channel positions.

LHCb Outer Tracker Internal Note

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Prepared by U.Uwer, D.Wiedner
Physikalisches Institut, University of Heidelberg, Germany
Antonio Pellegrino
NIKHEF, Amsterdam, The Netherlands

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1 Introduction

We will discuss the issue of addressing both for the Data and ECS. In the data stream, addresses can be found in:

1. OTIS ID in OTIS Headers (see [1]) ;
2. GOL ID in DAQ and L1 Headers.

In the ECS, there will be several addresses, depending on the exact configuration of the Control Paths; here we will deal only with the I²C addresses of the OTIS[1] and GOL[2] chips on the FE Electronics.

For clarity, it was chosen to use a geographical scheme for the addresses, even though this gives a larger address space than a progressive serial scheme. In order to identify geographically the OTIS and GOL in the FE Electronics, we need to identify:

- a) the OT Station: ST1, ST2, ST3 (2 bits)
- b) the Layers in each station: X, U, V, X (2 bits)
- c) the Quarters of each layer (2 bits)
- d) the 9 Modules in each quarter (4 bits).

In the I²C Control, only the 9 Modules need to be geographically identified, since each Quarter of each Layer has its own I²C bus.

2 OTIS ID in Data

In the following it is assumed that future versions of the OTIS TDC [1] will have 7 independent I²C address pins and 12 independent ID pads.

The 12 ID bits are sent with the OTIS header for every event. They are unique for every OTIS. Table 1 shows the OTIS ID containing OTIS number, module, quarter, layer and station. Please note that at least two address bits are non zero and the address should not be 11111111 1111, facilitating the synchronization on the OTIS header. ¹

Address bit	device	possible values
0-1	OTIS 0-3	00-11
2-5	module 1-9	0001-1001
6-7	quarter	00-11
8-9	layer	00-11
10-11	station	01-11

Table 1: OTIS address for OTIS header

3 GOL ID in data

The GOL address mentioned here will be generated on the L1 read out board (the GOL I²C address is defined in 4). ² It will be sent with every event to the L1 trigger and the DAQ. As 10 bits are necessary for a detector-wide unique GOL address, the scheme in table 2 is suggested here.

4 7 bit I²C address

The detector houses 24 service boxes on the four corners of each half station. To each service box two I²C busses are connected, one per layer. The I²C serial bus supplies slow control signals to the OTIS TDC and GOL 1.0 (and optional further components in the service box). Therefore, in each I²C bus,

¹The synchronization of the OTIS data on the L1 off-detector electronics board relies on finding the OTIS header starting with the 12 bit OTIS ID (MSB first) or a transport header consisting of 0xFF

²Please note that in the context of this address scheme only nine (out of 12) optical links will be connected to one L1 buffer board in the case of the Outer Tracker, corresponding one quarter of one layer.

Address bit	device	possible values
0-3	module 1-9	0001-1001
4-5	quarter	00-11
6-7	layer	00-11
8-9	station	01-11

Table 2: GOL address for L1 and DAQ

only the 9 Modules need to be geographically identified (4 bits), and, in each module, 6 devices (3 bits).

The 7-bits I²C addressing scheme in table 3 shows that the I²C address space available on one bus (7 bit address) is enough for the components on 9 detector module halves (4 OTIS + 1 GOL each), plus eventual additional I²C nodes on the service box. Each OTIS uses only one I²C address, while the GOL uses two consecutive I²C addresses (for pointer and data).

Bits [0-1] are used to choose one out of four OTIS chips on an auxiliary board. Bit 2 is used to choose between GOL (1) or OTIS (0). Bits [3-6] are used to select the module location. As the I²C protocol reserves address 0 to 7 and 120 to 127 for system calls (broadcasts), they must not be used as device address. Therefore:

- The module locations go from 0001 through 1001
- the remaining address space 1010-1110 can be used on the service box.

These 7 bits will be set on the GOL/AUX Board[3] and sent to the devices. The 4 MSBs of this address shall be set via a switch (“Module location address”); the three LSBs identifying the devices shall be hardwired. On the OTIS board, the common address bits for I²C and OTIS header ID will be wired together, so an OTIS will have the same address for the DAQ and the slow control.

5 Global location address

All address schemes introduced in previous sections follow a more general scheme, the “global location address”. Introducing a unique address convention facilitates the commissioning and operation of the Outer Tracker. The global location address is made up by:

Address bit	device	possible values
0-2	OTIS0	000
	OTIS1	001
	OTIS2	010
	OTIS3	011
	GOL pointer	100
	GOL data	101
3-6	module 1-9	0001-1001
	broadcasts	0000 and 1111
	service box	1010-1110

Table 3: I²C addresses

- channel
- (OTIS) chip
- module
- quarter
- layer
- station

All other addresses should follow the geographical scheme of global address. Figures 1 and 2 illustrate the geometrical mapping of the global address scheme, as we propose it:

- Inside one module channels are counted (looking from the module ends) from left to right for the lower halves and from right to left for the upper halves. This means counting always from left to right during straw installation and testing of half modules.
- The OTIS are counted as described in [3], the top right OTIS being number 0.
- The modules are counted from outside to inside the detector in order to have a symmetric layout and to ensure that physical identical modules get the same module number in both quarters.
- The address for the quadrants is chosen in a way to have one bit for upper/lower quarter and one bit for left/right.

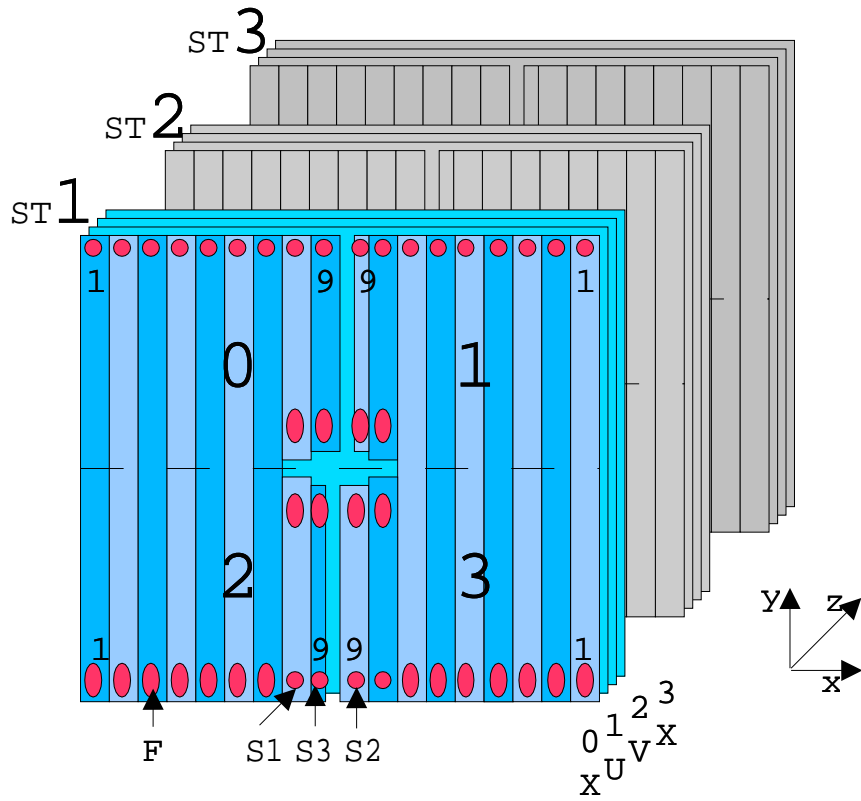


Figure 1: Global address for stations, quarters, layers, modules. Numbers are decimal for better overview.

- The layers go from 0 to 3 for each station, counting up down the beam.
- The station ID is counted from 01 upwards to avoid too many zeros in address headers.

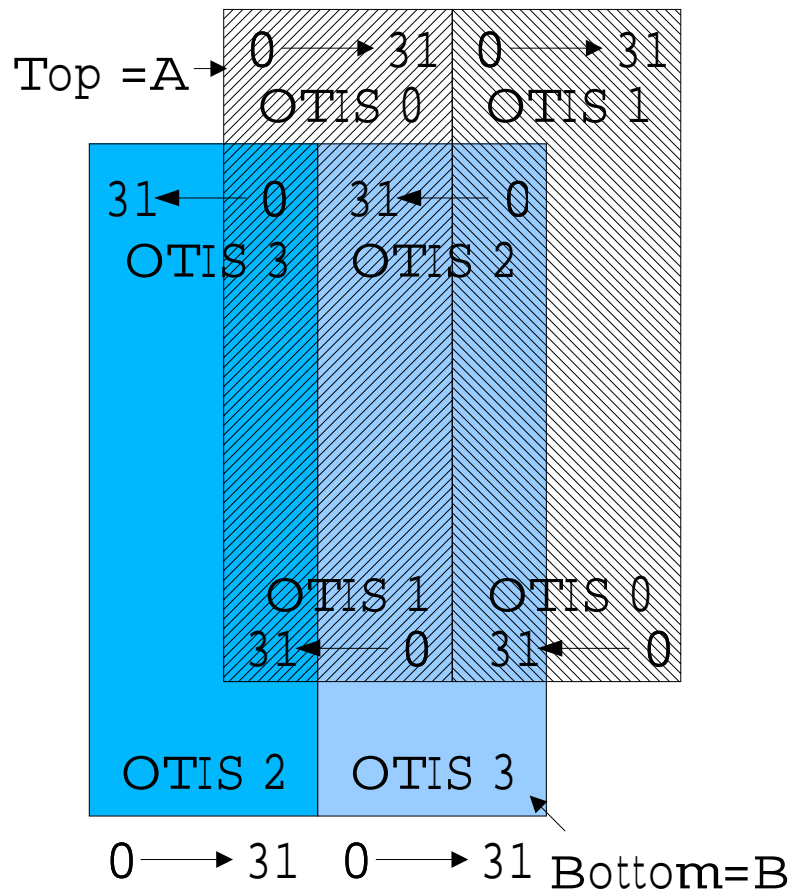


Figure 2: Address scheme inside one module. Numbers are decimal for better overview.

References

- [1] OTIS Reference Manual 1.0 , Harald Deppe, Uwe Stange, Ulrich Trunk, Ulrich Uwer
- [2] P.Moreira et al., GOL Reference Manual, Gigabit Optical Link Transmitter manual <http://proj-gol.web.cern.ch/proj-gol/manuals.htm>
- [3] Auxiliary Board for the Outer Tracker, Ad Berkien, Tom Sluik, U.Uwer, D.Wiedner, Albert Zwart